

Serial ATA I/II Subsystems

v1.3

Features / Benefits

- 1.5/3.0Gbps
- Serial ATA I/II v1.0a compliant
- Gen1i, Gen1m, Gen2i, Gen2m compliant
- Host or Device applications
- 5700 ppm data tracking capability
- PHY Ready, Partial and Slumber Power saving/modes
- Supports Mobile Graphics Low-Power addendum
- Out of Band signal detection
- Align and Comma detection with alignment
- SATA-Compliant Rate Adjust FIFO
- Loopbacks as defined by SATA I/II c1.0a specifications
- 8B10B Encode/Decode
- BIST with multiple pattern generation capability and compare block
- Multiple error status signals
- IEEE1194.1 and 1194.6 DC and AC JTAG support

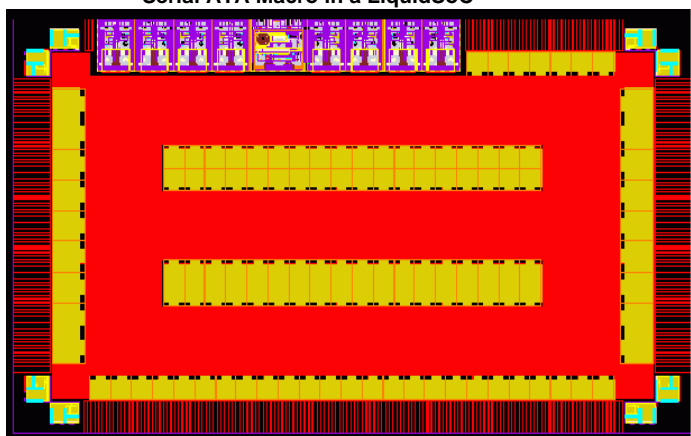
Applications

- Mass storage device
- Hard disk drives
- Optical drivers
- Computers

Product Description

The Rapid Bridge 1.5/3.0Gbps Serial Advanced Technology Attachment (SATA) I/II Serial Link PHY is suitable for host or device applications. This serial link is compliant with the Serial ATA I/II 1.0a specification, complies with Gen1i, Gen1m, Gen2i, and Gen2m specifications, and is Gen1x and Gen2x compatible. The PHY consists of a hardened Physical Media Attach (PMA) layer that is programmed to meet different system link budgets and configuration requirements, and a soft Physical Coding Sublayer (PCS) that is designed to be programmed for different applications and form factors. The PCS layer supports ALIGN detection and alignment, Comma detection and automatic detection of Out Of Band (OOB) signals. Different lane configurations from 1 to 32 lanes are available in the LiquidASIC offering. These may be further extended or modified to meet specific requirements in the LiquidSoC offering. A wide range of transmit amplitude and pre- and post- emphasis (de-emphasis), coupled with receiver equalization options, allow for optimum link budgeting of the overall system. The PIPE interface is programmable to 8 or 16-bits. A Clock and Data Recovery (CDR) circuit allows for different levels of filtering and loop bandwidths to accommodate ppm offset. This PHY also supports a Spread Spectrum Clock source. 8B/10B encoder and decoders are provided as part of the PCS layer to allow for full programmability and function extension. A wide range of reference clock inputs are supported to meet different system requirements and clocking schemes. SATA supports all power saving modes; PHY READY, PARTIAL and SLUMBER, in addition to SATA I/II 1.0a initialization and power-saving modes. This PHY incorporates a high level of built in test functions. It supports three different loopback modes: serial loop back, line-side loop back and parallel loop back. A centralized BIST consists of a pattern generator on the transmit side and a pattern verifier block on the receive side. Multiple patterns in support of different standards may be generated by the BIST block. The pattern verifier block aligns itself with the generated pattern and records number of mismatches in the captured data. This PHY also supports IDDQ testing and DC and AC JTAG in accordance to IEEE1149.1 and 1149.6.

Serial ATA Macro in a LiquidSoC™



Serial ATA I/II Subsystems

Complete Subsystem Solution

Rapid Bridge 1.5/3.0Gbps SATA I/II serial link PHY is part of the LiquidSerDes family and is offered as an integrated part of LiquidASIC and LiquidSoC platforms. This PHY provides a wide range of programmability to meet different system requirements. LiquidSerDes is register- and metal-programmable and benefits from a wide range of amplitude, pre- and post- emphasis and receiver equalization settings; this enables link optimization beyond a specific standard. This PHY may be operated at full, half and quarter rate, resulting in internal power optimization and wide range of reference clock selections. The parallel interface may be operated at 8, 10, 16 or 20 bits for different core signaling frequencies. This design also incorporates additional power-saving features, such as electrical idle detection at different signaling levels and beacon signaling. LiquidSerDes incorporates a comprehensive set of Built In Self Test (BIST) functions with multiple pattern and noise generation capabilities, which simplifies system validation. Internal BIST is complemented with different loopback capabilities, providing comprehensive fault coverage. Core boundaries utilize scan registers, and DC and AC JTAG are supported to allow for board-level continuity tests. SATA PHY is complemented with third-party transaction and link layers to meet users' specific system needs.

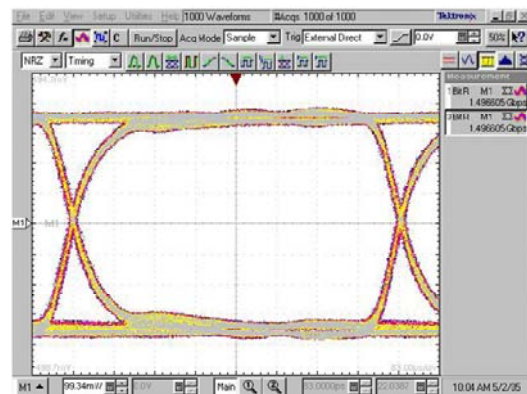
For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

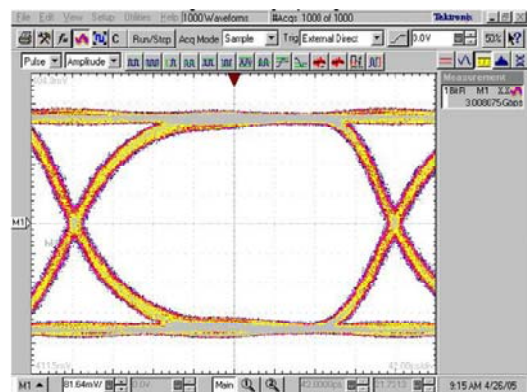
sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

This SATAI/II PHY is a tightly integrated subsystem that addresses the interaction of many interdependent parameters between different analog, mixed-signal and digital blocks. This approach yields a homogenous subsystem that provides optimum performance, power and area. Metal-programmability of this PHY further allows for architectural flexibility and feature enhancements that otherwise would not be possible. Different silicon characterization over PVT has been performed to eliminate any potential design weaknesses. LiquidSerDes meets ESD of 2kV HBM and 500 CDM as part of the LiquidASIC and LiquidSoC platforms.



1.5Gbps Transmitter Eye Diagram



3.0Gbps Transmitter Eye Diagram