

CEI-6 Short Range Subsystems

v1.2

Features / Benefits

- OIF 6.4G SR CEI-6 Compliant
- 1.06-6.4Gbps data rate
- Full, Half, and Quarter Rate options
- Less than 0.28UI jitter generation
- Adaptive Receiver equalization for enhanced jitter tolerance
- Amplitude and pre/post-emphasis options
- Eye width mapping and on chip jitter test features
- Power saving modes
- Signal detection
- ± 100 ppm offset
- 8-, 10-, 16-, 20-bit parallel interface
- 8B10B Encode/DecodeBIST circuitry with multiple pattern generation capabilities
- Multiple loopback test circuitries
- Multiple error status signals
- IEEE1194.1 and 1194.6 DC and AC JTAG support

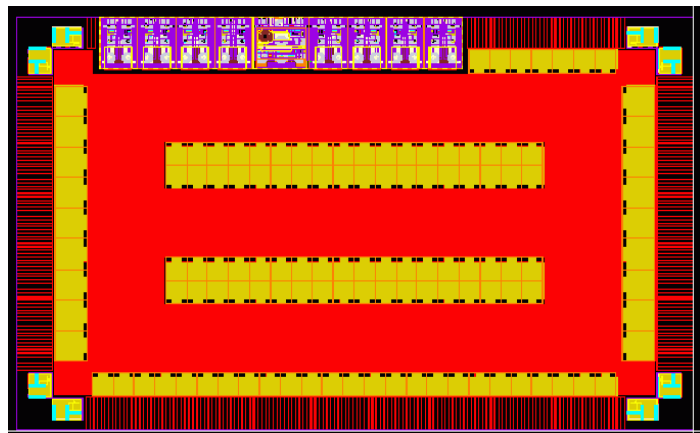
Applications

- Optical Network
- Backplane

Product Description

Rapid Bridge Common Electrical Interface CEI-6 is compliant with Optical Interworking Forum's (OIF) 6 Gbps short range specification. This architecture allows for full rate, half rate or quarter rate operations, for an operating data rate range of 1.06 to 6.4 Gbps. This PHY is comprised of a hardened Physical Media Attach (PMA) layer that is programmed to meet different system link budgets and configuration requirements, and a soft Physical Coding Sublayer (PCS) that is intended to be programmed for different applications and form factors. Multiple 4-lane configurations are available in the LiquidASIC offering. These may be further extended or modified to meet specific requirements in the LiquidSoC offering. Wide range of transmit amplitudes, pre and post emphasis (de-emphasis) coupled with receiver equalization options allow for optimum link budgeting of the overall system. PIPE interface is programmable to 8 or 16-bits. Clock and Data Recovery (CDR) circuit allows for different levels of filtering and loop bandwidths to accommodate ppm offset. This PHY also supports Spread Spectrum Clock source. 8B/10B encoder and decoders are provided as part of the PCS layer to allow for full programmability and function extension. A wide range of reference clock inputs are supported to meet different system requirements and clocking schemes. PCS layer also incorporates comma detection and word symbol alignment. This PHY incorporates a high level built in test functions. It supports three different loop back modes: serial loop back, line-side loop back and parallel loop back. A centralized BIST consists of a pattern generator on the transmit side and a pattern verifier block on the receive side. Multiple patterns in support of different standards may be generated by the BIST block. Pattern verifier block aligns itself with the generated pattern and records the number of mismatches in the captured data. This PHY also supports IDDQ testing and DC and AC JTAG in accordance to IEEE1149.1 and 1149.6. All receive and transmit on die terminations are automatically calibrated to ensure proper return loss across the frequency spectrum. Architecture of this PHY results in low level of jitter generation that is well below the IEEE802.3a requirements for both deterministic and sinusoidal jitter components.

CEI-6 Macro in a LiquidSoC™



CEI-6 Short Range Subsystems

Complete subsystem Solution

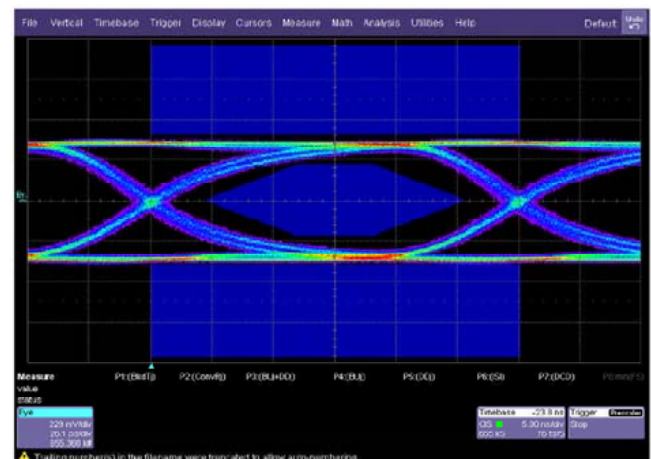
Rapid Bridge Common Electrical Interface 6 serial link PHY is part of LiquidSerDes family and is offered as an integrated part of LiquidASIC and LiquidSoC platforms. LiquidSerDes PHY provides wide range of programmability that allows users to meet different system requirements. LiquidSerDes is register and metal programmable and benefits from a wide range of amplitude, pre and post emphasis and receiver equalization settings that allows for link optimization beyond a specific standard. This PHY may be operated at full, half or quarter rate, resulting in internal power optimization and a wide range of reference clock selections. Parallel interface may be operated @ 8, 10, 16 or 20 bits for different core signaling frequencies. This design also incorporates additional power saving features such as electrical idle detection at different signaling levels and beacon signaling. LiquidSerDes incorporates a comprehensive set of Built In Self Test functions with multiple pattern and noise generation capabilities that simplifies system validation. Internal BIST is complemented with different loop back capabilities providing comprehensive complete fault coverage. Core boundary utilize scan registers and while DC and AC JTAG are supported to allow for board level continuity test.

Performance Beyond the Past

Rapid Bridge CEI-6 serial link is a tightly integrated subsystem that addresses the interaction of many interdependent parameters between different analog, mix-signal and digital blocks. Different silicon characterizations over PVT have been performed to eliminate any potential design weaknesses. LiquidSerDes meets ESD of 2kV HBM and 500 CDM as part of LiquidASIC and LiquidSoC platforms.



Stressed Receiver Jitter Tolerance



For More Information. . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

TX Compliance Eye Mask Test