

## RLDRAMII Subsystems

v1.2

### Features / Benefits

- 400 - 1066 Mbps
- 576/288 Mb x9/18 /36 configurations
- 1.8V/1.5V operation
- Impedance calibrated 50/75/150Ω ODT
- Calibrated output impedance of 18Ω with half strength option
- Clock synchronization and boundary alignment on the read operation
- ¾ latency on during write cycle
- Programmable read latency for wide range of system implementation.
- Optional pipe insertion at the controller interface for ease of timing
- Integrated master and slave DLL with supply regulation and resolution of up to 10 ps.
- Programmable delayed address and command lines
- Fully programmable within Rapid Bridge LiquidASIC and LiquidSoC
- Micron MT49HXXX RLDRAMII Compatible

### Applications

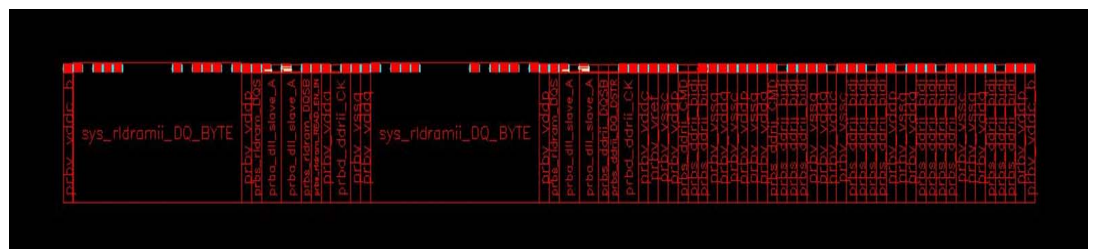
- RLDRAMII Memory Interface

### Product Description

Reduced Latency DRAMII is a high performance memory that is intended for networking and cache applications. RLDRAMII differs from the standard DDRII SDRAMs by incorporating a free running output data clock (QK). RLDRAMIIs are offered in Common IO (CIO) types. In the CIO type devices, read and write ports are shared and an additional cycle is required for bus turnaround. The CIO devices are intended for data streaming, in which near-term bus operation is either 100% read or write, independent of the long term balance.

Rapid Bridge platform incorporates a unique, patented architecture that allows for systematic implementation of Reduced Latency DRAMII memory subsystems. Worst case physical layer write latency is ¾ cycle. Read Latency is programmable to allow a wide range of system implementations while maintaining low latency. Different RLDRAM memory system configurations can be realized or altered through metallization to support data rates from 400 to 1066 Mbps and different configurations. Physical layer (PHY) can be complemented with Northwest Logic memory controller, or other controllers maybe used, to provide a comprehensive solution with seamless implementation. This PHY incorporates feature sets that simplify the overall communication to different SDRAMs. On Die Termination (ODT) and impedance calibrated output drivers ensure optimum termination and signal integrity. An optional core side pipeline stage simplifies the controller and PHY interface. Regulated master and slave Delay Lock Loops with metal programmable range and resolution simplify the top level link budgeting of the interface.

An integrated multi-phase PLL allows for ½ clocking rate that improves the overall power consumption of the logic section. The power consumption is further enhanced by providing half strength drive options and matched calibrated pull up and pull down drivers. The address and command lines may be pipelined and delay controlled to optimize the timing of the interface and load requirements. The serialization is done through ping-ponging of the clock using different phases, thus minimizing write latency to ¾ of pipeline while improving the DQ/DK(B) link budget at the top level. Multiple options are provided at the read interface to allow for trade offs between read latency, operating frequency and system requirements.



RLDRAMII 576Mb x36-bit PHY with embedded PLL/DLL

## RLDRAMII Subsystem

### Complete subsystem Solution

RLDRAMII subsystem is part of the LiquidPHY family providing a comprehensive System on Chip platform that is designed with a homogeneous and systematic approach that yields optimum power, area and speed. These subsystems are comprised of LiquidIO, LiquidMXS and LiquidCell foundation LiquidIPs, specifically defined to address the functionality and performance of the LiquidPHY.

LiquidPHY subsystems benefit from all the advantages of foundation LiquidIPs, such as metal programmability, testability, integration, yield, ESD, etc.

These subsystems address many difficult to solve integration issues that cross boundaries between analog, digital, and mix-signal realms associated with electrical characteristics and physical design implementation. They significantly reduce engineering design cycle time, and eliminate potential risk.

In most cases LiquidPHY subsystems are complemented with their respective MAC, PCS or other controller blocks, which are made available as hard or soft macros to allow for further customization. Different physical configurations of the LiquidPHYs are available as hardened blocks.

These configurations may be used as-is or further modified to meet the physical requirements of the top level system. All LiquidPHY subsystems are provided with simulation models that closely model the analog and mix-signal blocks for accurate modeling of the system.

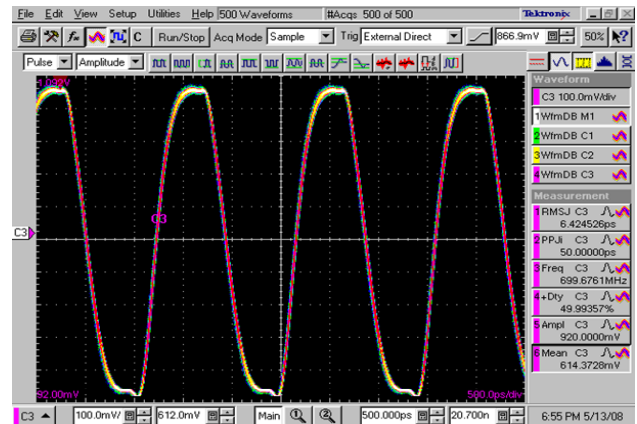
### For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit [www.rapidbridge.com](http://www.rapidbridge.com)

### Performance Beyond the Past

The RLDRAMII LiquidPHY is a tightly integrated subsystem that addresses the interaction of many interdependent parameters between different analog, mix-signal and digital blocks. This approach yields a homogenous subsystem that provides optimum performance, power and area. The metal programmability further allows for architectural flexibility and feature enhancements that otherwise would not be possible.



Clock Output @ Ouput Waveform @ @ 1.4Gbps, silicon results