

Master/Slave DLL A/B/C/D

v1.2

Features / Benefits

- 200-1400Mbps
 - A: 200-700Mbps
 - B: 350-850Mbps
 - C: 750-1050Mbps
 - D: 800-1400Mbps
- 7-bit, 128 stage delay elements
- Resolution of 8 to 16ps
- <4mW power dissipation
- DLL lock function
- Regulated supply voltage for high supply noise rejection
- IDDQ, scan and bypass modes
- Metal programmable within Rapid Bridge platform

Product Description

Master and Slave Delay Lock Loop family is intended for source synchronous interface applications where eye-centering is required. Master DLL determines a 7-bit code that correspond to 90° phase offset based on a reference clock. 7-bit code is transmitted to Slave DLLs that in turn convert the code to a respective delay equaling the 90° phase shift. Slave DLL may be inserted in an open loop path and provided eye-centering. Master and Slave architecture is intended for DDR applications and is applicable to continuous or non-continuous strobe signaling. Both Master and Slave delay element operate on regulated supply that are also configured as master and slaves for accuracy and incremental regulation based on the interface width and requirements. Master and Slave DLL are used in composition of higher level LiquidPHY subsystems such as DDR1/II/III, QDRI/II, GDDR3/IV, RLDRAM1/II, PCI_X, RTBI etc.

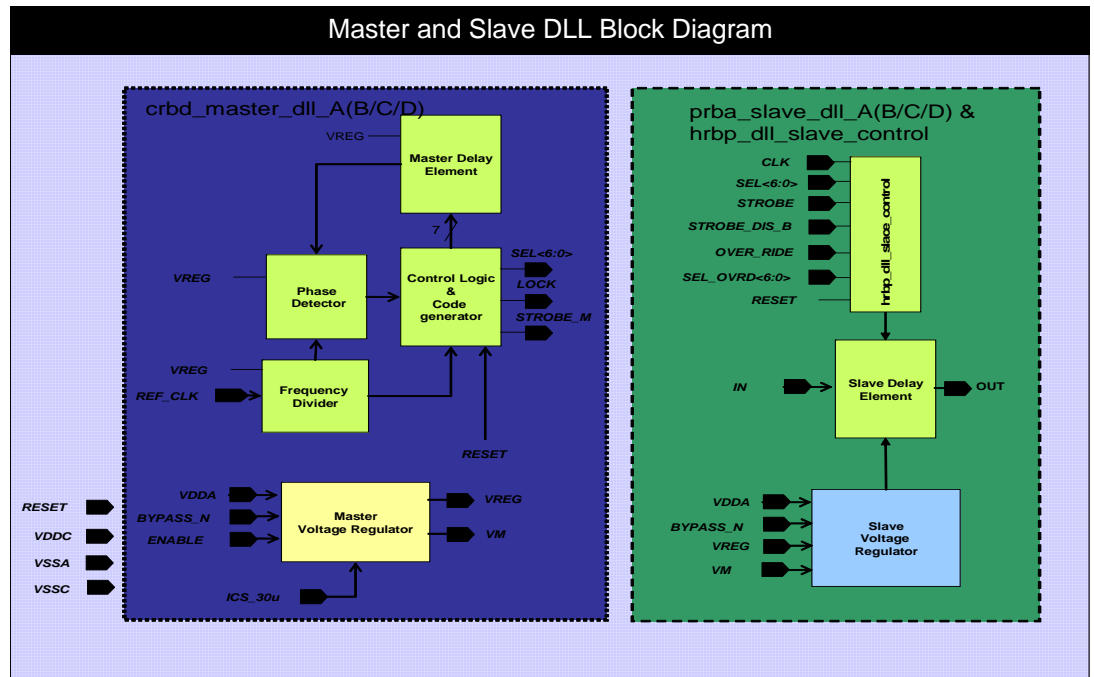
An SoC Approach

LiquidMXS is integrated along with LiquidIO and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.

Applications

- Interface timing blocks requiring eye-centering
- Continuous or non-continuous strobing
- DDR1/II/III
- QDRI/II
- GDDR3/IV
- RLDRAM1/II
- PCI, PCI_X
- RTBI, TBI
- RGMII, XGMII

Master and Slave DLL Block Diagram



Master/Slave DLL A/B/C/D

Complete Timing Block Solution

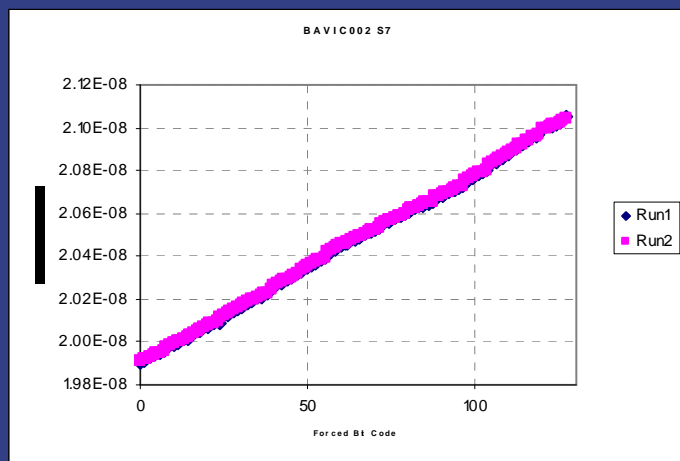
PLL and DLL solutions provide a wide range of performance timing blocks which are tailored for different types of applications. These PLLs and DLLs may serve as frequency synthesizers, de-Skew PLLs, Interface PLLs with multiple phases, and high resolution DLLs for tight timing budgets. Specific jitter parameters are tuned within each family to address specific application requirements.

Master and Slave DLLs are implemented with IDDQN, DLL_EN and SCAN_EN functions to allow for test and validation of the DLL and the SoC as a complete system. Guidelines have been followed in design and layout to minimize the effect of different sources of noise for optimum performance. Application guidelines are provided within SoC chip and in COT environment to ensure proper integration and performance.

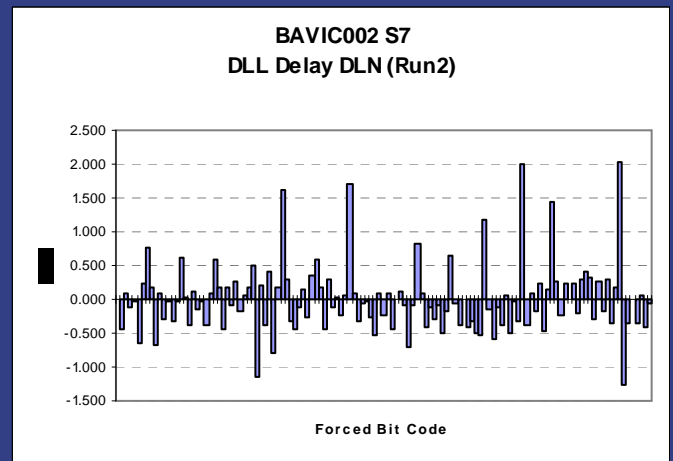
Performance Beyond the Past

Definition and composition of the different PLL and DLL types is under the umbrella of a complete sub-system definition. The holistic approach in definition, design implementation, physical design and integration result in silicon efficiency that can not be realized through other approaches and results in optimum performance and amortization of analog and Mix-Signal resources available at the chips level. This approach also eliminates so difficult to manage integration issues at the SoC level minimizing potential risks.

Silicon results of the DLL delay vs. code



Silicon results of the DLL D DNL



For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com