

Low Voltage TTL (LVTTTL) IO Cell

v1.2

Features / Benefits

- EIA/JESD 8B narrow, normal and wide range compliance
- Multiple drive strength; 2/4/8/12mA
- Up to 150MHz operation
- Calibrated push/pull driver
- Logic programmable pull up and pull down structures
- IDDQ, parametric Nand and JTAG test functions
- Multiple slew rates
- Metal programmable within Rapid Bridge™ platform
- 35µm pad pitch
- ESD 2kV (HBM)
- Wirebond and Flip Chip versions available
- IEEE 1149.1 Compliant

Applications

- General purpose interface
- Mobile SDRAM interface
- CellularRAM Memory interface

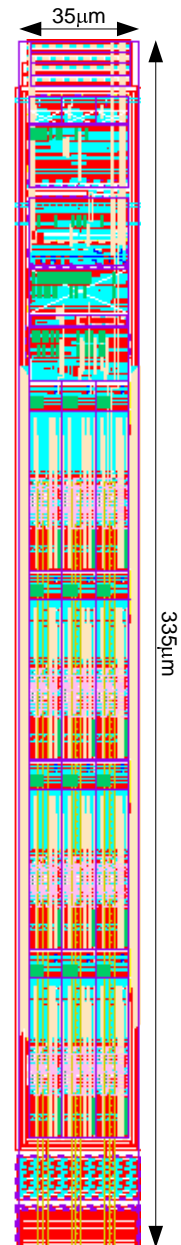
Note: LVCMOS IO provide better performance than the 3.3V LVTTTL and should be used in <2.75V environments

Product Description

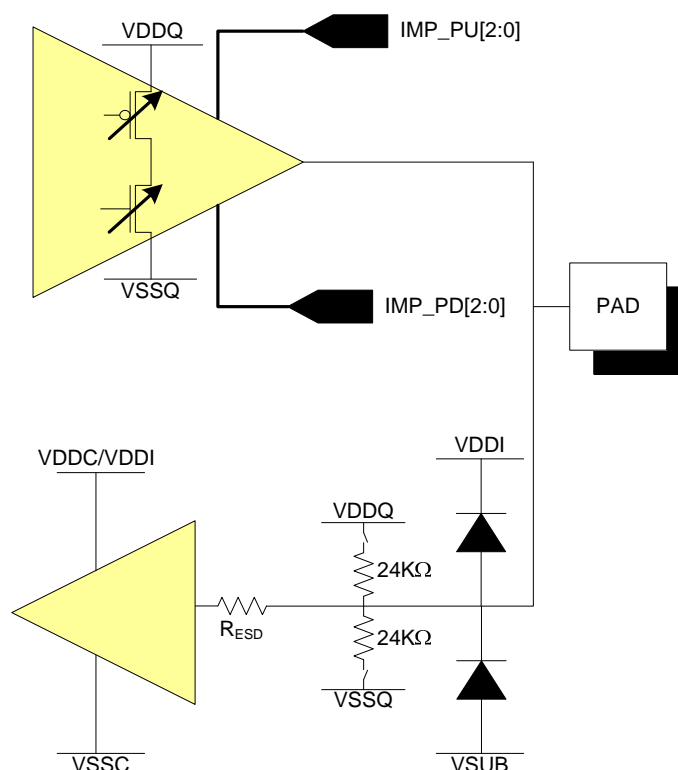
Low Voltage TTL is a 3.0-3.6V unterminated IO interface targeted for low performance, low cost general purpose applications. LVTTTL IO set provides pads with drive strengths from 2 to 12mA in order to meet different application requirements beyond those specified by EIA/JESD 8B. Core programmable 24kΩ pull up and pull down structures eliminate the need for external components.

An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



LVTTTL Block Diagram



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Complete Interface Solution

GDDRIII interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design.

IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. System level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

GDDRIII is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. Systematic implementation of LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

Silicon results for TTL @ 500 and 20MHz, no load

