

# LVPECL IO Cell

v1.2

## Features / Benefits

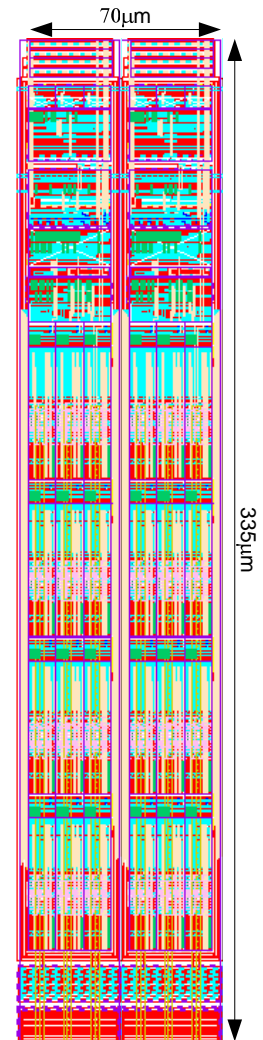
- Programmable output current 8/12/14/18mA
- Up to 750MHz operation
- Open Drain architecture
- No external bias required.
- IDDQ, parametric Nand and JTAG test functions
- Metal programmable within Rapid Bridge platform
- ESD 2kV HBM, 200V MM, 500V CDM
- True Differential input, output, and bidirectional versions.
- 3.3 or 2.5V VDDQ
- Output can be terminated to multiple standards
- Less than ±3% duty cycle distortion across PVT
- Wirebond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

## Product Description

Low Voltage Positive Emitter Coupled Logic (LVPECL) is a technology-independent interface that may be designed into a variety of integrated circuit technologies. An open-drain architecture along with a programmable steering current allows different system implementations. The interface may be run at 3.3V or 2.5V to allow further system flexibility and several common mode requirements. The LVPECL interface is intended to operate at frequencies up to 750MHz (1.5Gbps). LPECL is interoperable with other standards such as HSTL, LVDS, and CML. This IO may be also AC coupled into dc-balanced systems to accommodate different common mode requirements. Multiple steering currents enable adjustable differential signaling levels, which are needed for power and noise margin optimization. When properly terminated, the constant driver current produces a fixed current in the link as well as the driver, which in turn simplifies system design by eliminating supply switching current surges.

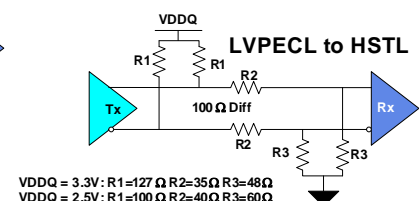
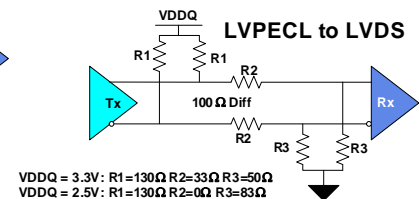
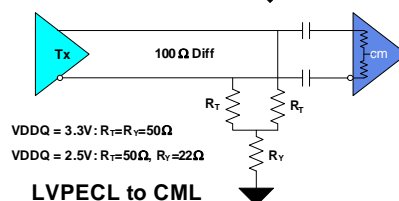
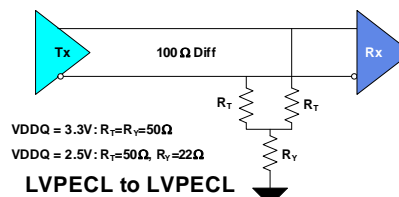
## An SoC Approach

LiquidIO is integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. Readily integrated subsystems addresses many challenges and concerns associated with high speed interface designs.



## Applications

- SGMII interfaces
- General Purpose signaling
- High speed serial clocking
- Networking, RAMlink, SPI4
- Backplane, graphics displays



## LVPECL IO Cell

### Complete Interface Solution

LVPECL interface is part of a complete IO ring solution, that has been specifically designed for high performance, easy chip integration, and flexible system level requirements. This top-level integrated IO design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. IOCalculator software is a WEB based tool that allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. RingComposer is used to compose the entire ring and the respective support circuits based on output of the IOCalculator. Test functions are composed and are correct by construction. System level ESD results in better than 2kV HBM, 200V MM and 500V CDM models. Combination of the above tool sets and metal programmability creates a complete liquid infrastructure allowing full flexibility and re-programmability.

### For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit [www.rapidbridge.com](http://www.rapidbridge.com)

### Performance Beyond the Past

LVPECL is part of a harmonious system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top level system requirements. Reduction in power is coupled with well matched and balanced output impedances that enhances signaling and performance throughout the system. The systematic implementation of the LiquidIO subsystem eliminates potential, difficult to address, interface interactions.

### Silicon results of LVPECL trceivers, 1.4GHz clock

