

GTL / GTLP IO Cell

v1.3

Features / Benefits

- JESD8-3 compliance
- Up to 150MHz data rate
- Independent dynamic pull up and pull down calibration
- Open Source architecture
- IDDQ, parametric Nand and JTAG test functions
- Multiple logical implementations to simplify system composition.
- Less than $\pm 3\%$ duty cycle distortion across PVT
- $35\mu\text{m}$ / $70\mu\text{m}$ pad pitch
- ESD 2kV HBM, 200V MM and 500V CDM
- 1.5/1.2V signaling
- Wire-bond, Flip Chip and CUP versions available
- IEEE 1149.1 Compliant

Applications

- Backplane applications for heavily loaded lines

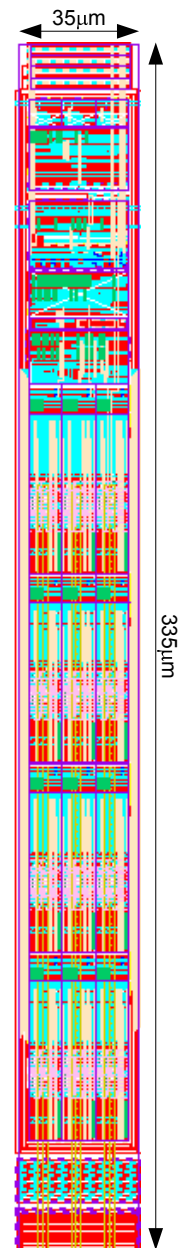
Product Description

Gunning Transceiver Logic (GTL) and GLT Plus (GTLP) are reduced-swing IO drivers intended to facilitate high-speed busses on backplanes. Open-source architecture requires external termination and may be tri-stated to allow for different bus structure implementations. GTL/GTLP interface is governed by JESD 8-3. It is intended to operate at frequencies up to 150MHz with a load of 30pF and a termination resistance of 25Ω into 1.2V or 1.5V for GTL and GTLP, respectively. Output impedance is calibrated to minimize current and output low voltage variation across PVT, eliminating the need for over-design at the package and board level to address high switching currents. This IO is intended for point-to-point as well as multi-drop bus applications.

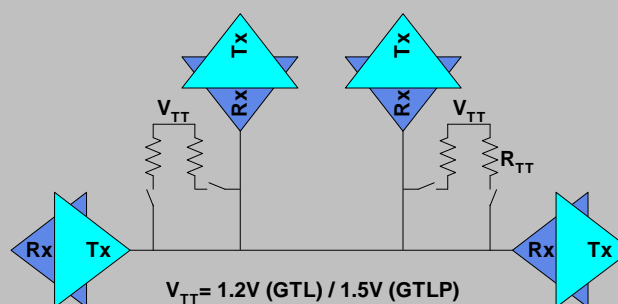
Receiver's voltage reference is set to 0.8V and 1.0V for GTL and GTLP, respectively. Higher output voltage swing of the GTLP in general results in increased noise margin.

An SoC Approach

LiquidIO is ideally integrated along with LiquidMXS and LiquidCell to create highly integrated, efficient and comprehensive LiquidPHY subsystems. These readily-integrated subsystems address many challenges associated with high-speed interface designs.



GTL/P sample multi-point termination



GTL / GTLP IO Cell

Complete Interface Solution

GTL and GTLP interface is part of a complete IO ring solution, which has been specifically designed for high performance, easy chip integration, and flexible system-level requirements. This SoC design approach eliminates redundant components, such as multiple bias generation and calibration circuits, and prevents power supply fragmentation, leading to smaller area, lower power utilization, and better ESD protection. System-level ESD results in better than 2kV HBM, 200V MM and 500V CDM models.

Because the IOs are designed to work together, test methodology has been greatly simplified as well. Parametric Nand trees, JTAG scan chains, and IDDQ testing can all be accomplished with minimal circuits and control lines.

Proprietary software available from Rapid Bridge may be used to help create correct-by-construction IO rings with mixed IO types and the proper number of support pads for a successful design. This software allows end users to calculate power pad requirements based on packaging and system specifications for the supported standard within the Rapid Bridge LiquidIO family. It can also be used to compose the entire ring and the respective support circuits based on power requirements. Test functions are composed and are correct by construction.

The combination of the above tools and metal programmability creates a complete “liquid” infrastructure that allows full flexibility and re-programmability.

For More Information . . .

Regarding LiquidIP™, LiquidASIC™, or LiquidSoC™, please contact Rapid Bridge at:

sales-support@rapidbridge.com or visit www.rapidbridge.com

Performance Beyond the Past

GTL/P is part of a harmonious SoC system that is calibrated through a Central Calibration Unit across process and temperature. This yields significant improvement in rms and peak currents of up to 60%, reducing top-level system requirements. This reduction in power is coupled with well-matched and balanced output impedances that enhance signaling and performance throughout the system. A systematic implementation of LiquidIO subsystem eliminates the most difficult-to-address interface interactions.

GTL / GTLP results

